High-Performance Bipolar Transistors with SiGe:C and Poly-SiGe

The performance of silicon-based high-speed bipolar transistors has greatly improved over the last few years. Recently, a transistor with a record cut-off frequency of 210 GHz was presented by IBM [1]. The basis of this technology is an epitaxially grown SiGe base, making it possible to engineer the band gap and achieve a narrower base than ever before. The inevitable boron out-diffusion from the base layer can be minimized by the addition of carbon.

Because of its relative simplicity, non-selective epitaxy is commonly used for this type of device. One drawback is the subsequent non-self-aligned patterning of the layers necessary to build up the emitter and the connections to the base [1, 2]. So far, only a rather complicated process flow has been demonstrated, which includes conversion of poly-Si to oxide for the manufacture of self-aligned transistors from a non-selective epitaxially grown base [3].

Another approach starts with a selectively grown base layer in the emitter window [4]. However, selective epitaxy is known to suffer from severe loading effects. This means the epitaxial parameters will need to be tuned for each layout with a different device density. Moreover, the selective process is very difficult to control, which easily leads to voids and poor base contacts.

A common problem in all self-aligned double-poly processes is related to the subsequent removal of the silicon used for the extrinsic base inside the emitter opening without etching down into the underlying monocrystalline silicon. This becomes more severe for a process involving an epitaxial base: since the base layer is formed prior to the emitter window etch as opposed to a process where the base formed by ion implantation through the etched emitter opening. Many solutions have been suggested in literature. In the case of SiGe-based non-selective epitaxy, the etching problem has recently been addressed [5]. Here, a boron silicate glass (BSG) layer was used both as an etch stop and as a diffusion source for the electrical link-up between the external and the internal parts of the base.

This article is based on a recently presented conference paper [6]. All SiGe-depositions have been performed in a Unaxis SIRIUS™ UHV-CVD system. The modular concept used for the extrinsic base can also be applied to a more conventional double-poly bipolar process flow which uses an implanted base.

Device manufacture

The fabrication of the device follows an earlier process scheme up to the formation of the collector contact [7]. A nitride and silicon seed layer are then deposited and patterned prior to a non-selective SiGe:C epitaxy of the intrinsic base. This is followed by the deposition of a bi-layer of poly-SiGe and poly-Si for the extrinsic base layer. Before the deposition of an oxide, the extrinsic base region is implanted with a high dose of boron. The implanted boron will later be out-diffused, thereby forming the extrinsic base connection. The stack is then patterned and etched to form the emitter window. Subsequent processing follows a conventional double-poly bipolar process flow. A schematic cross-section of the resulting transistor is shown in Figure 1.

Intrinsic base module details

The intrinsic base was grown in a Unaxis SIRIUS™ UHV-CVD system. The depositions were made at a working
Extrinsic base module details

After the intrinsic base was grown, poly-SiGe with about 30% Ge was deposited at low-temperature in the UHV-CVD system. The deposition started with a thin Si seed layer in order to facilitate the nucleation of the subsequent poly-SiGe film. Then a 500 Å thick poly-SiGe film with 30% Ge was deposited and capped with a thin Si layer. AFM analysis of the poly-SiGe film showed the surface roughness was about 60 Å in the active and the field areas.

The extrinsic base was completed by the deposition of a 600 Å thick poly-Si film using an ordinary LP-CVD furnace. Subsequently, the poly-Si layer was implanted with $2 \times 10^{15}$ cm$^{-3}$ of BF$_2$ at 35 keV. Finally, the extrinsic base stack was covered by a deposited oxide layer.

The emitter window was opened by dry etching of the isolation oxide, followed by an etch of the poly-Si and poly-SiGe layers using an HBr/Cl$_2$ based chemistry. Using the system monochromator, the 3040 Å emission line from the etch plasma was used to indicate the location of the interface between poly-Si and poly-SiGe. The endpoint of the etch was triggered by the signal reaching maximum intensity. Timed etching was then used to etch through the poly-SiGe layer, stopping at the underlying Si epitaxial layer.

Figure 3: XSEM of the emitter window after a timed etch of the poly-SiGe film

An XSEM (cross-sectional scanning electron micrograph) of the emitter opening after the timed poly-SiGe etch is shown in Figure 3. The uniformity of the extrinsic baseetch across the wafer was found to be excellent and no loading effects could be detected.

Figure 4: XSEM of the transistor after HF treatment as recorded in the backscattered mode

Figure 2: XTEM of the non-selective epitaxy
Tungsten plugs and SiGe films are seen as bright layers. It has been reported the oxidation rate of SiGe is enhanced by a factor of three compared to Si, and that Ge segregates to the interface of the growing oxide [8]. However, the poly-Si layer which covered our poly-SiGe film protected the latter from oxidation during the densification of a sacrificial oxide layer on the base.

The poly-Si covering the poly-SiGe layer also facilitated the titanium self-aligned silicide process in the metallization step; the poly-Si was thick enough to prevent the formation of a thermally unstable germano-silicide.

No difference in sheet resistance was observed between a standard Ti silicidation of Si and the silicided poly-Si/poly-SiGe film stack.

**Electrical measurements**

The current quality of the manufactured transistors is demonstrated in Figure 5, which shows a Gummel plot for a single transistor with an emitter area of 0.4 x 10 µm² at a base-collector voltage of 0.1 V. The collector currents display ideal characteristics which indicate that the epitaxial base layer is dislocation free. The relatively low collector saturation current, extracted from the single transistor, is due to an out-diffusion of boron from the SiGe layer into the Si substrate. For the single transistor, the base current is ideal over several decades of current. A peak value of about 100 can be extracted for the current gain. Figure 6 shows the extraction of fT = 53 GHz and fmax = 80 GHz for a single device. Although fmax is considerably higher than fT, which indicates a good extrinsic base formation, the fT can be increased further by optimization of the base-collector region.

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**References**


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**Figure 5:** Gummel plot for a single transistor with an emitter area of 0.4 x 10 µm²

**Figure 6:** Extraction of fT and fMAX for a fabricated device